What is claimed is:

1. A circuit comprising:

at least one phase lock loop to generate at least one core signal having multiple cycles within one cycle of an external signal;

a ratio decoder to decode a programming code; and

an alignment unit coupled to the at least one phase lock loop and the ratio decoder to synchronize a plurality of propagation pulses with the external signal based on the programming code.

2. The circuit of claim 1, wherein the alignment unit includes a master pulse generator to generate a master pulse having a pulse width equal to one cycle of the at least one core signal.

3. The circuit of claim 1, wherein the alignment unit includes a propagation pulse generator to periodically provide each of the propagation pulses to an propagation compensator of the alignment unit at a propagation interval before an occurrence of an anticipated edge of the external clock.

4. The circuit of claim 3, wherein the propagation pulse generator includes a counter and a reset unit coupled to the counter to reset the counter after a first propagation pulse among the plurality of propagation pulses is generated.

5. The circuit of claim 1, wherein the ratio decoder includes a math unit to perform a math operation on the programming code.

6. The circuit of claim 5, wherein the ratio decoder further includes a selector to select between a control value represented by a programming code and a control value resulted from the math operation.

7. An integrated circuit comprising:

a phase lock loop network to receive an external signal to generate at least one core signal;

a master pulse generator to generate a master pulse based on a combination of the at least core signal and a modified version of the external signal;

a propagation pulse generator coupled to the master pulse generator to generate a plurality of propagation pulses based on the master pulse;

an propagation compensator coupled to the propagation pulse generator to propagate the plurality of propagation pulses for a propagation interval to generate an internal clock signal; and

a ratio decoder coupled to the propagation pulse generator to provide at least one control value to influence a timing of the plurality of propagation pulses.

8. The integrated circuit of claim 7, wherein the master pulse generator includes a logic unit to enable a pulse width of the master pulse to be one cycle of the at least one core signal.

9. The integrated circuit of claim 8, wherein the master pulse generator further includes a reset unit to reset the master pulse generator.

10. The integrated circuit of claim 7, wherein the propagation pulse generator includes a counter coupled to the master pulse generator.

11. The integrated circuit of claim 10, wherein the counter is a ring counter.

12. The circuit of claim 7, wherein the ratio decoder includes a logic circuit to perform a subtraction operation on the at least one control value.

13. The circuit of claim 12, wherein the ratio decoder further includes a selector to select the at least one control value.

14. The integrated circuit of claim 7, wherein the propagation compensator includes a plurality of flip-flops coupled in series between an output node of the propagation pulse generator and an output node of the propagation compensator.

15. The integrated circuit of claim 7 further comprising at least one component coupled to the propagation compensator to receive the internal signal.

16. A system comprising:

a clock generator to generate an external signal;

a dynamic random access memory device coupled to receive the clock generator; and

a plurality of integrated circuits coupled to receive the external signal, at least one of the plurality of integrated circuits including:

an internal signal generating unit to generate at least one core signal;

a ratio decoder to decode a programming code; and

an alignment unit coupled to the internal signal generating unit and the ratio decoder to synchronize a plurality of propagation pulses with the external signal based on the programming code.

17. The system of claim 16, wherein the internal signal generating unit include multiple phase lock loops coupled in a cascaded configuration.

18. The system of claim 16, wherein one of the integrated circuit includes a processor.

19. The system of claim 16, wherein the alignment unit includes a master pulse generator to generate a master pulse having a pulse width equal to at least one cycle of the at least one core signal.

20. The system of claim 16, wherein the alignment unit includes a propagation pulse generator to periodically provide each of the propagation pulses to an propagation compensator of the alignment unit at a propagation interval before an occurrence of an anticipated edge of the external clock.

21. The system of claim 16, wherein the ratio decoder includes a logic unit to perform a math operation on the programming code.

22. The system of claim 21, wherein the ratio decoder further includes a selector to select between a control value represented by a programming code and a control value resulted from the math operation.

23. A method comprising:

generating a core signal based on an external signal, the core signal having core cycles;

producing a master pulse based on a combination of the core signal and a modified version of the external signal;

producing a plurality of propagation pulses including a first propagation pulse and a group of subsequent propagation pulses, wherein the first propagation pulse is produced at an initial interval after the master pulse is produced; and

propagating the plurality of propagation pulses for a propagation interval to align the plurality of propagation pulses with the external signal.

24. The method of claim 23 further comprising setting a reference value, wherein the reference value represents a number of the core cycles within one cycle of the external signal.

25. The method of claim 23, wherein the master pulse having a pulse width, wherein the pulse width equals an interval between two consecutive rising edges of the core signal.

26. The method of claim 23, wherein the initial interval is a variable value.

27. The method of claim 23, wherein the propagation interval is an interval between an occurrence of one of the propagation pulses and an occurrence of an anticipated edge of the external clock signal.

28. The method of claim 23, wherein the initial interval includes a number of initial core cycles, wherein a number of initial core cycles is less than a number of core cycles within one cycle of the external clock signal.

29. The method of claim 28, wherein each of the subsequent propagation pulses is produced at a multiple of the number of core cycles within one cycle of the external clock after the first propagation pulse is produced.